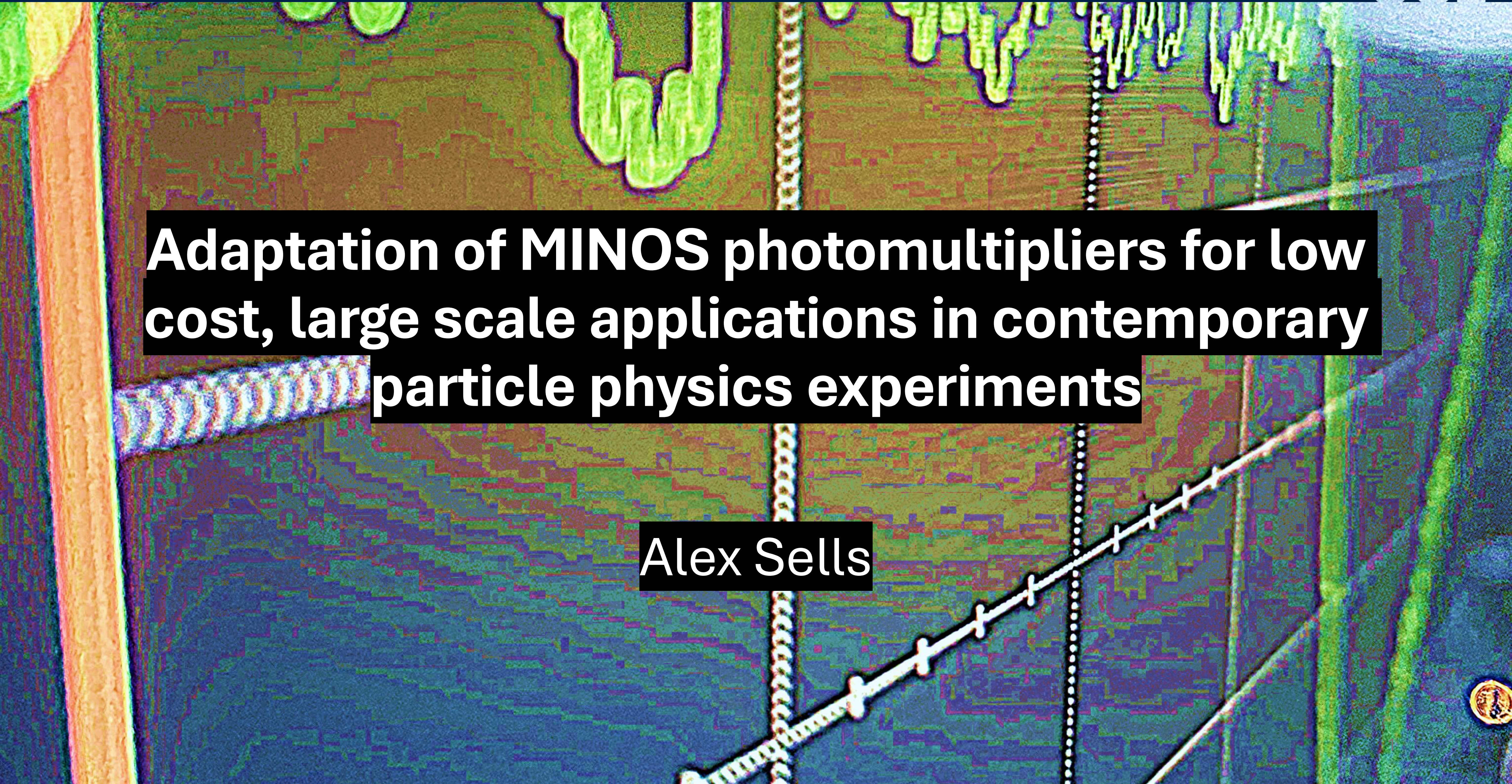
UCL

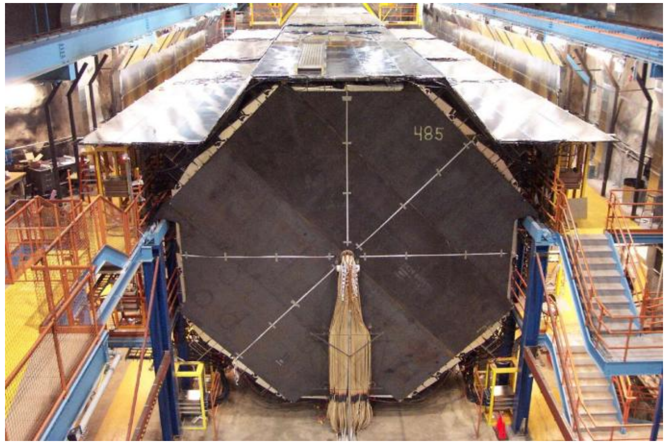


Adaptation of MINOS photomultipliers for low cost, large scale applications in contemporary particle physics experiments

Alex Sells

The MINOS experiment

- MINOS: long-baseline experiment measuring ν_μ disappearance from 2005 – 2016
- Detected ν interactions at a near detector close to the NuMI beam, and a far detector 735km away
- Detectors consist of alternating steel and scintillator strip planes, monitored by 1550 ‘M16’ Hamatsu PMTs (Far) and 215 ‘M64’ PMTs (near)
- Many of these are now not in use – 1000s of light channels



Electronics for modern applications

- Modern neutrino experiments are larger, with higher numbers of detector photo-channels
- One potential limiting factor is the HV required to power PMTs
- HV cable, safety infrastructure and generators are expensive, especially distributed over a wide area
- The CHIPS detector, an economical neutrino detector concept, aimed to address this problem in its electronics design

After CHIPS

- Principles of CHIPS project - to create economical light detection system continue in R&D program
- PMTs used to develop easily deployable DAQ node system with GPS synchronized timing using WR project technology

‘DAQ node’ – mains powered bespoke electronics

28x

WIPAC
Wisconsin IceCube Particle Astrophysics Center

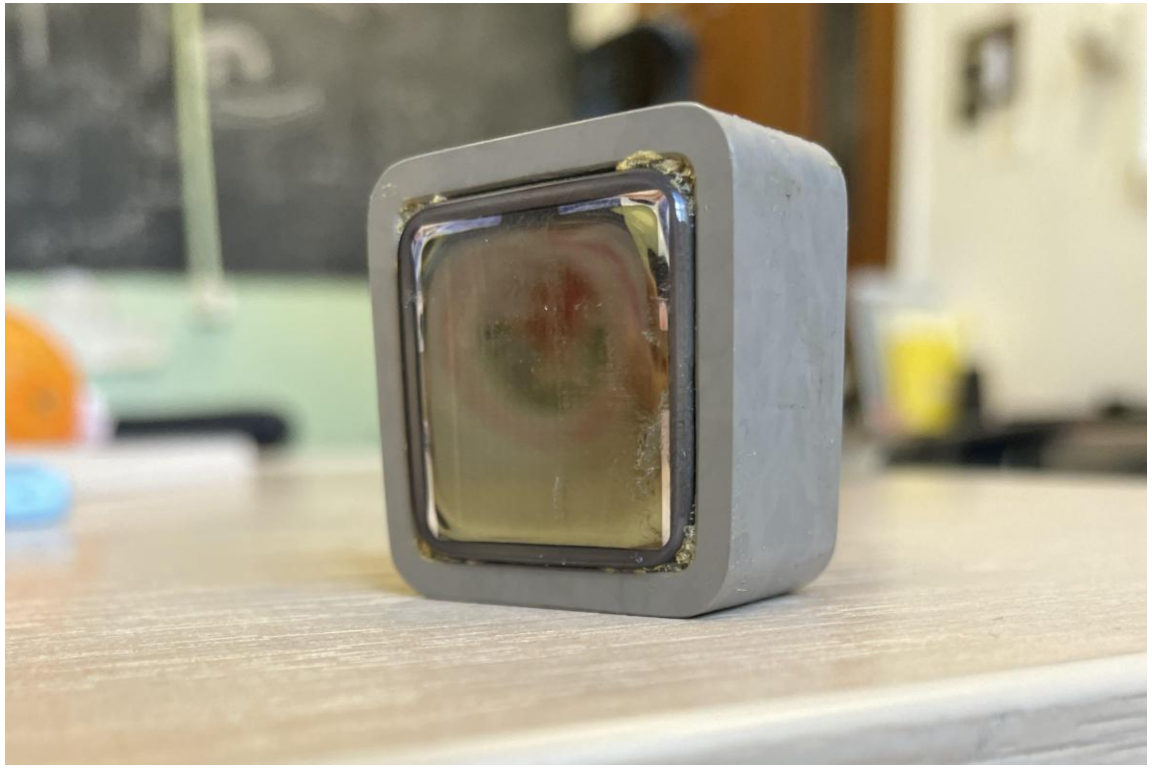
Stacked ‘micro-DAQ’, Cockroft-Walton powerbase and R6091 PMT

Taking cosmic ray data in London, Prague, Quy Nhon (Vietnam)

White Rabbit Project technology – uses internet and satellite GPS for global time synchronization to <10ns

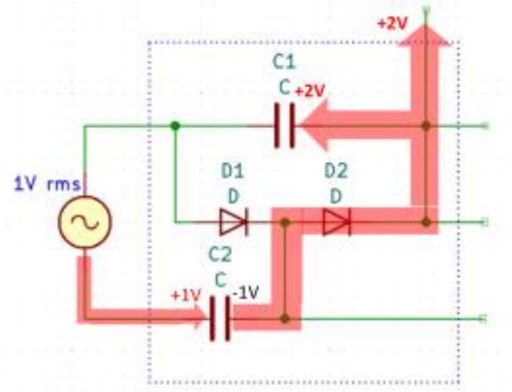
Hamamatsu M64

- Hamamatsu R5900-00-M64 is a 64 anode metal channel dynode photomultiplier (PMT)
- Photocathode is ~3x3cm
- Operational voltage 800 – 1000V
- Low level light detection (single photon), suitable for variety of different environments

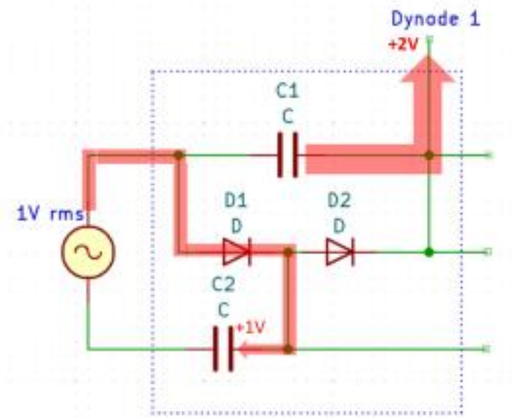


Cockroft Walton Voltage Multiplier

- Series of voltage multiplier stages that each provide a potential difference of twice the AC input
- Output is rectified to DC
- A sequence of stages can produce very high voltage from relatively low input voltage



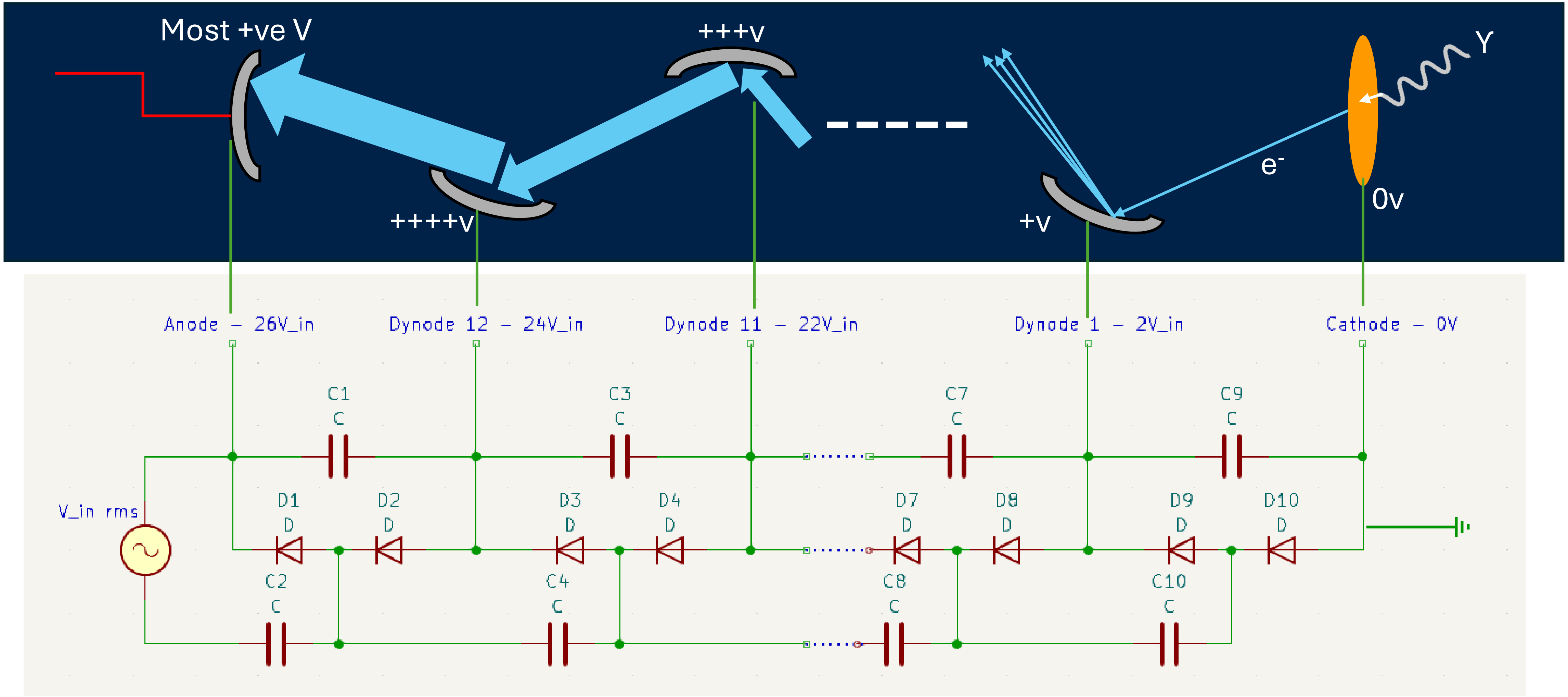
(b) C2 discharges and with the source provides twice the voltage



(c) As C2 recharges, C1 discharges to maintain output

The two phases of a voltage multiplier circuit

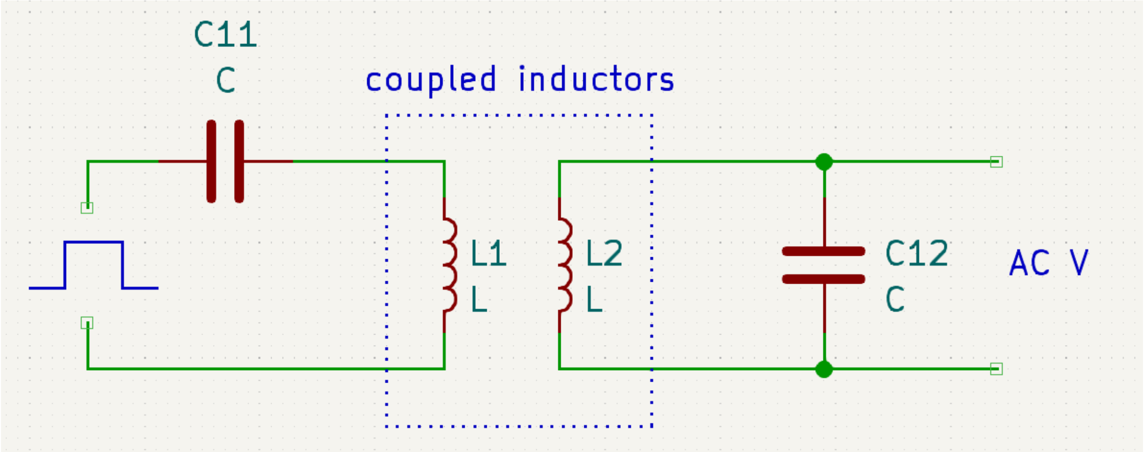
M64 powerbase

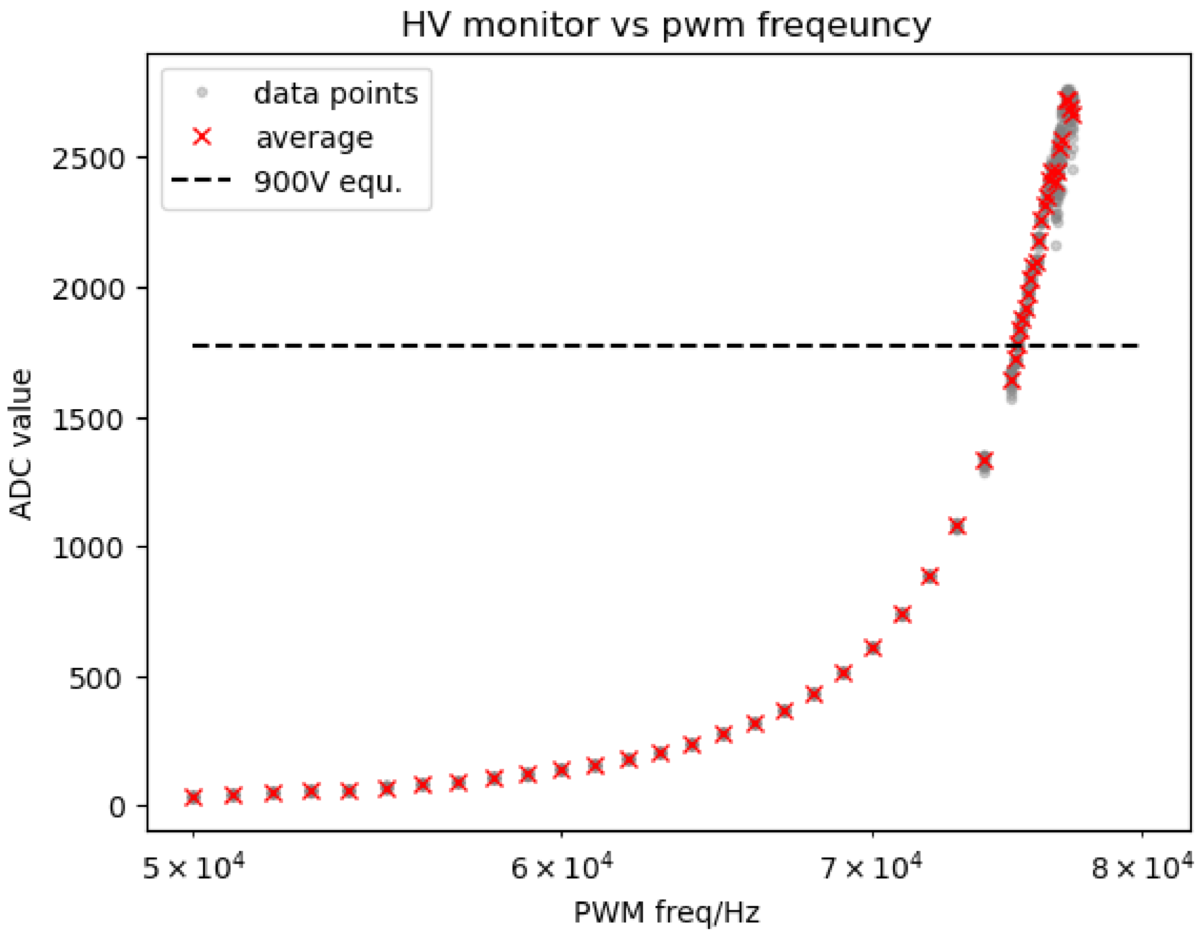


[1]Positive polarity Cockroft Walton PMT powerbase: COUPP experiment; Crisler, M. et al., 2010, October. The Chicagoland Observatory Underground for Particle Physics cosmic ray veto system. In IEEE Nuclear Science Symposuim & Medical Imaging Conference (pp. 808-812). IEEE.

PWM HV Control

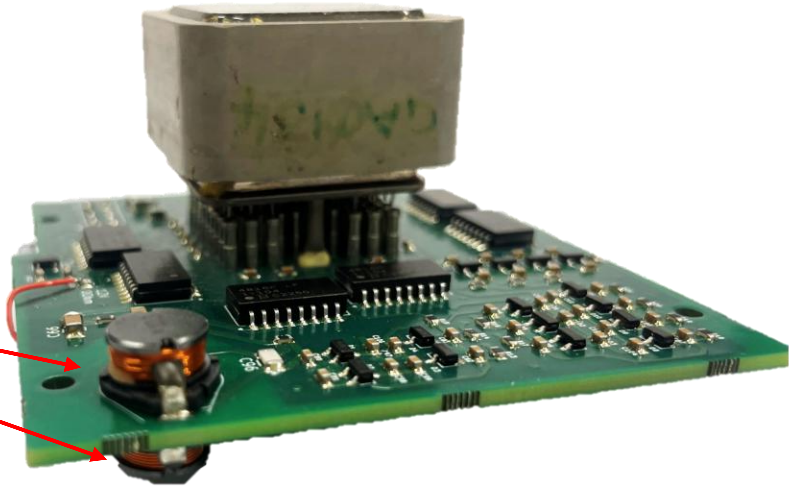
- Input AC to Cockroft Walton comes from resonant transformer
- Frequency used to control HV level
- Transformer decouples HV and suppresses harmonic noise



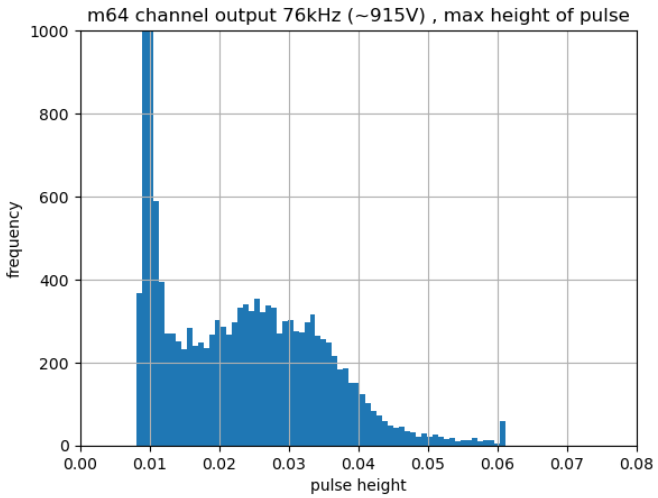


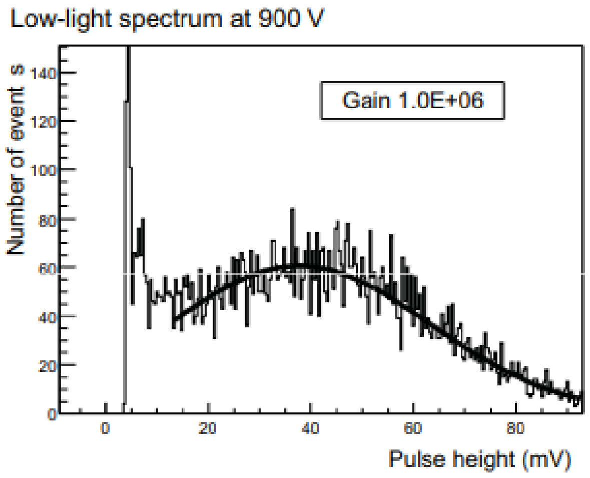
Design of powerbase

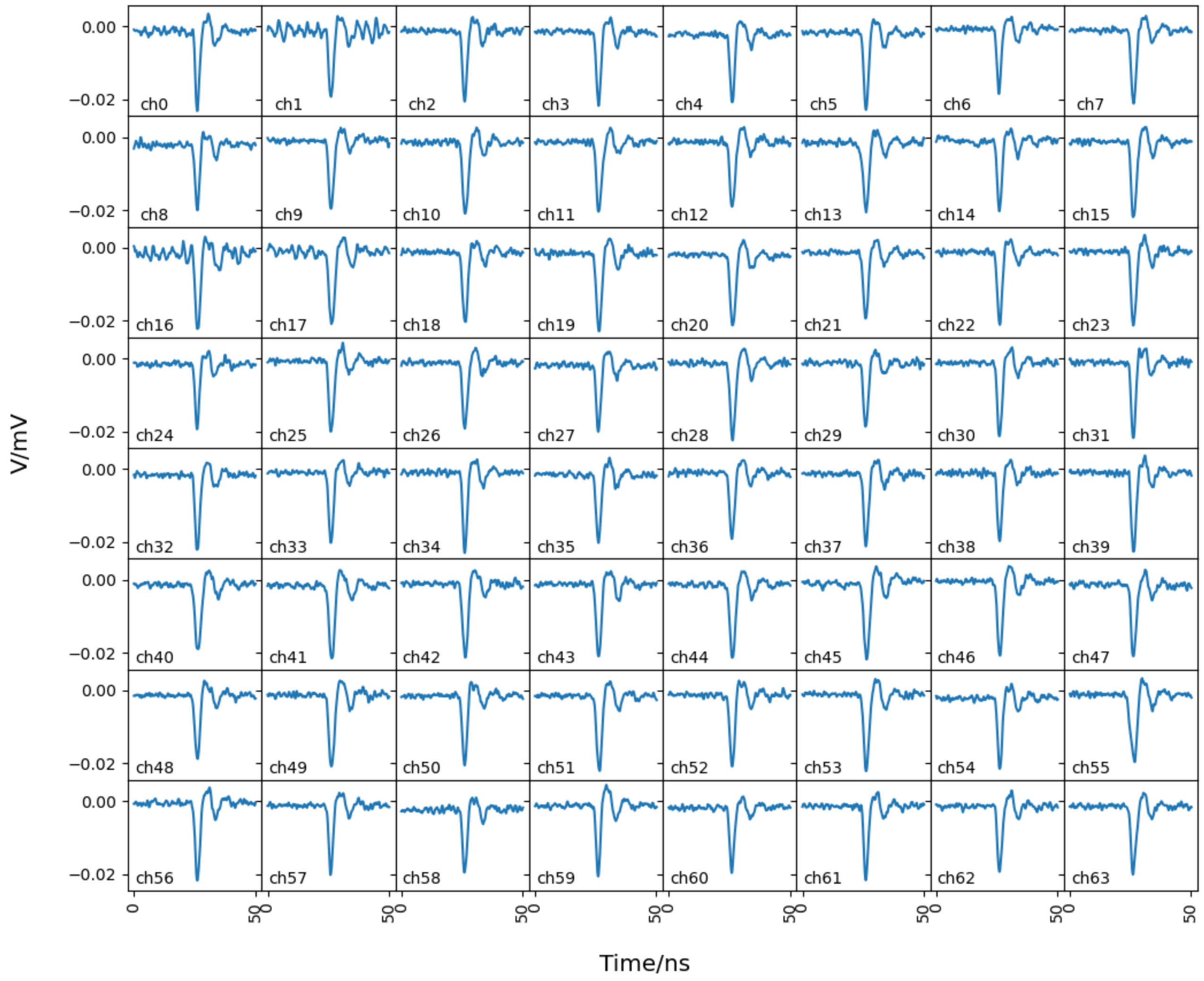
- Standard digital 3.3V PWM signal as input
- ‘LC tank’ uses the resonance of an inductor and capacitor to shape the input and increase its amplitude
- 15 stage Cockroft Walton Chain connected to the dynodes
- ADC for voltage monitoring connected to an untapped CW stage
- All relatively low cost, commercially available components



Performance

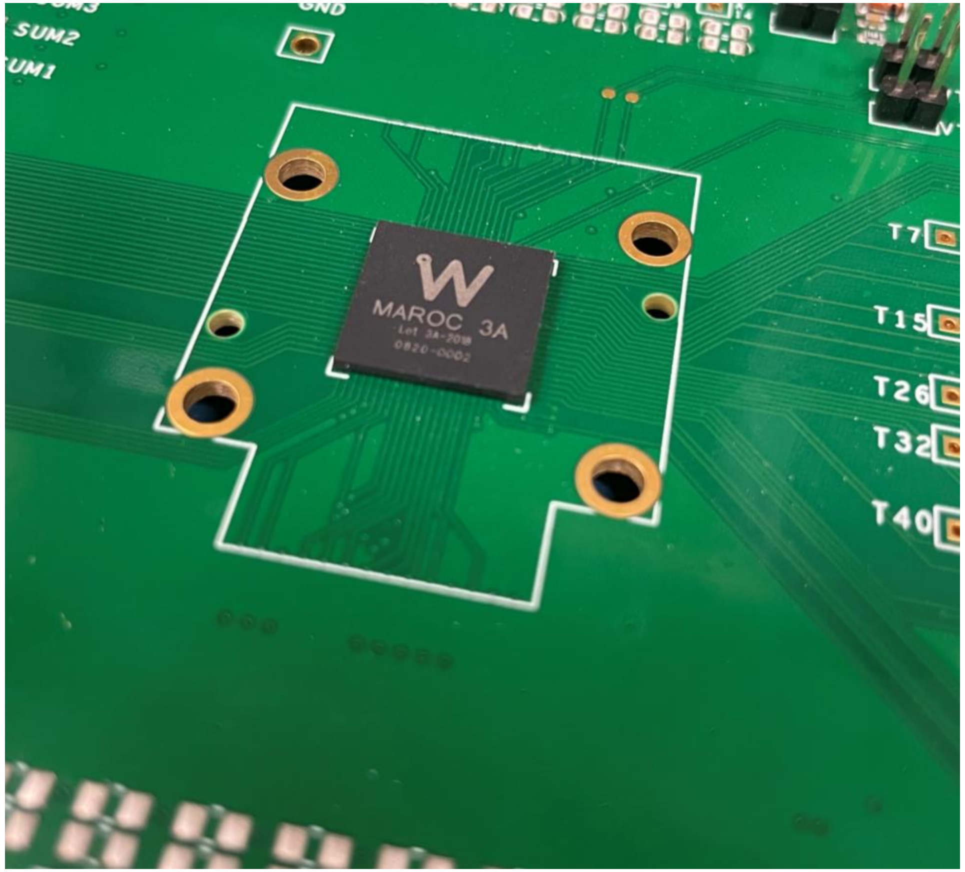






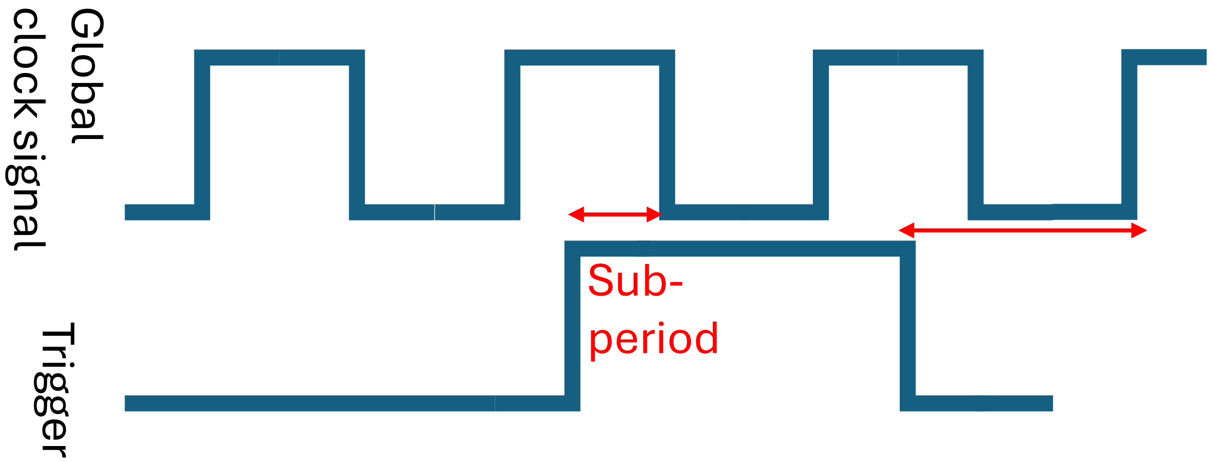
Readout – The MAROC3A

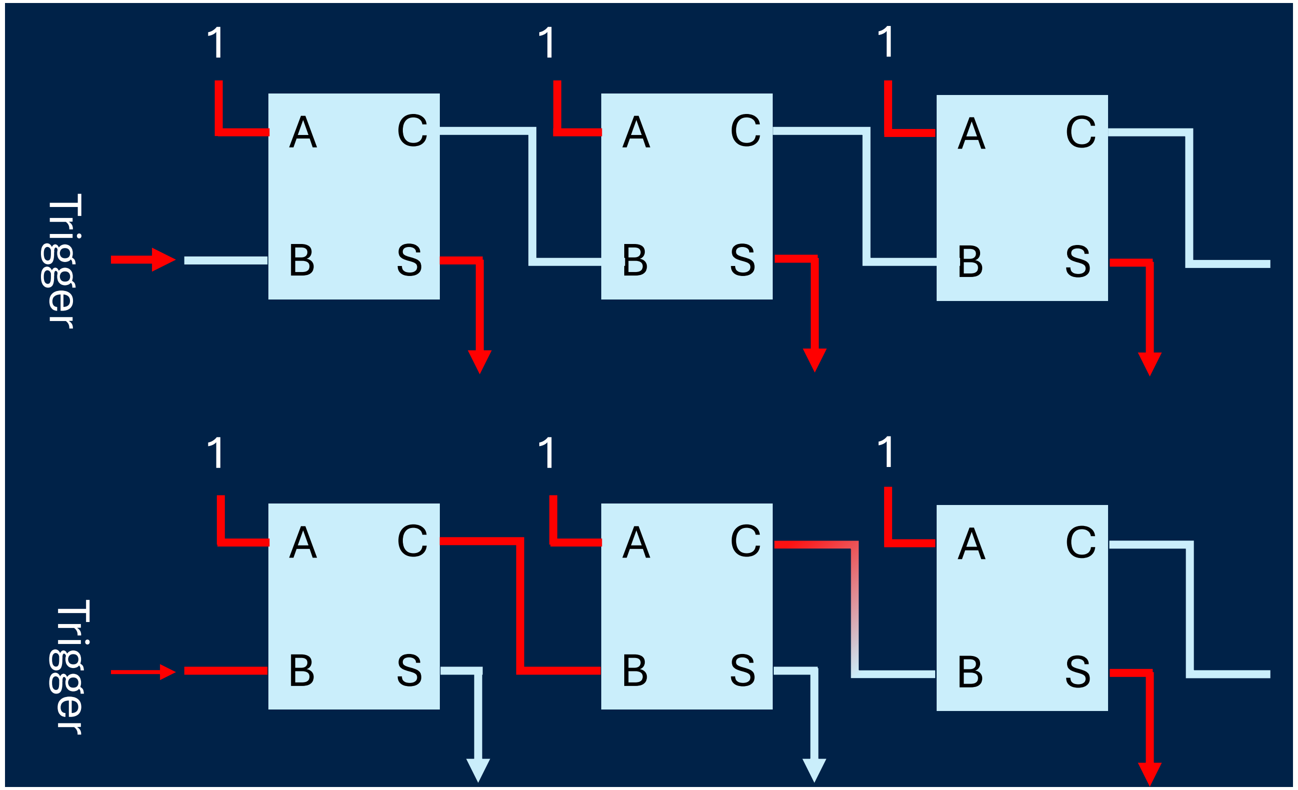
- Version of readout chip designed for ATLAS ‘Roman Pot’ detectors
- Readout chip designed for multi-anode PMTs, with 64 channels ideal for M64
- Provides individual channel gain settings, pulse discrimination, charge measurement – all in one



Tapped Delay Lines

- Implemented Tapped delay lines in FPGA
- Allow for division of clock period
- Course time period of 2.105ns, sub-nanosecond time over threshold resolution





See: Wang, Yonggang, et al. "Performance analysis and IP core implementation of two high performance time-to-digital converters on Xilinx 7-series FPGA." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1020 (2021): 165866.

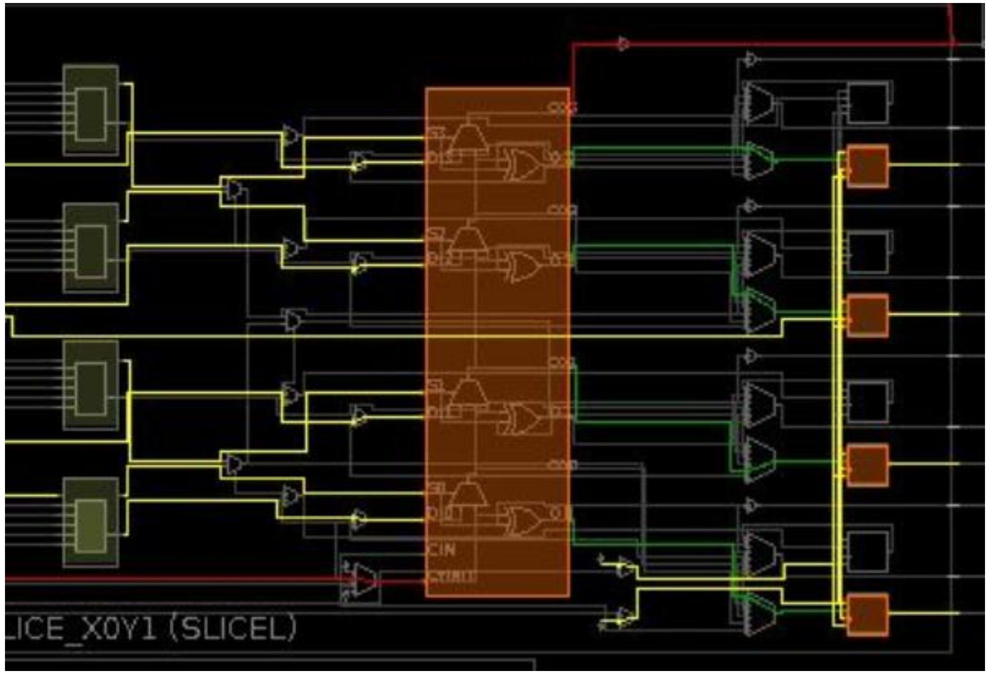
Architecture

- Deploying FPGA TDC based on design by Parsakordasiabi et al. (2021) [2]
- Architecture optimised for low resource usage ideal for 64x channels
- Built on Genesys 2 FPGA with AMD Kintex™ 7 XC7K325T-2FFG900C
- 475MHz clock and maximum ~200 carry chain operations per TDL

[2]Parsakordasiabi, Mojtaba, et al. "A low-resources TDC for multi-channel direct ToF readout based on a 28-nm FPGA." *Sensors* 21.1 (2021): 308.

TDL Calibration

- Tiny manufacturing inconsistencies mean that the time between carry logic operations is not equal
- We can run statistical ‘code density’ test to find the true width of each TDL stage

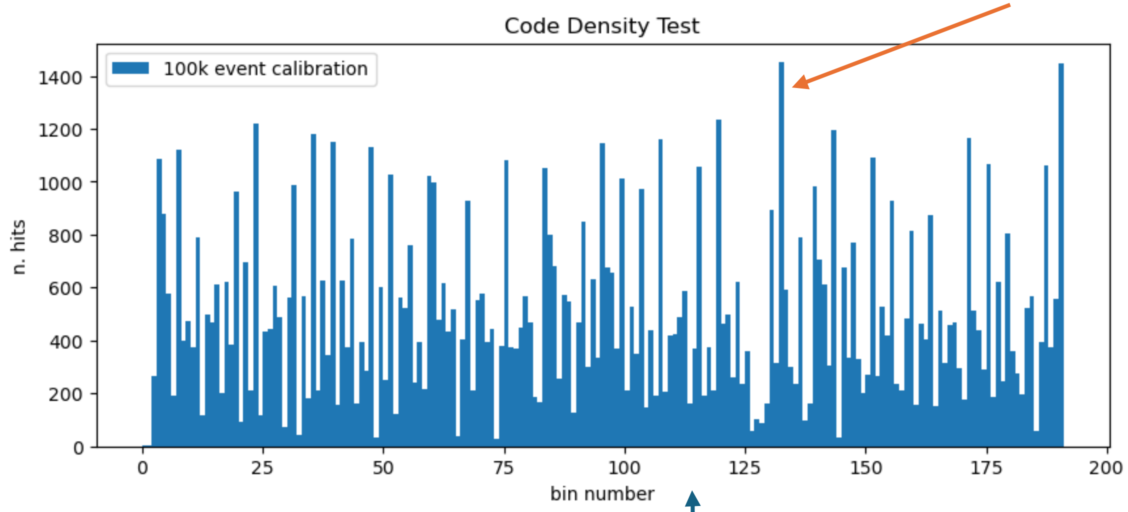


Parsakordasiabi, Mojtaba, et al. "A low-resources TDC for multi-channel direct ToF readout based on a 28-nm FPGA." *Sensors* 21.1 (2021): 308.

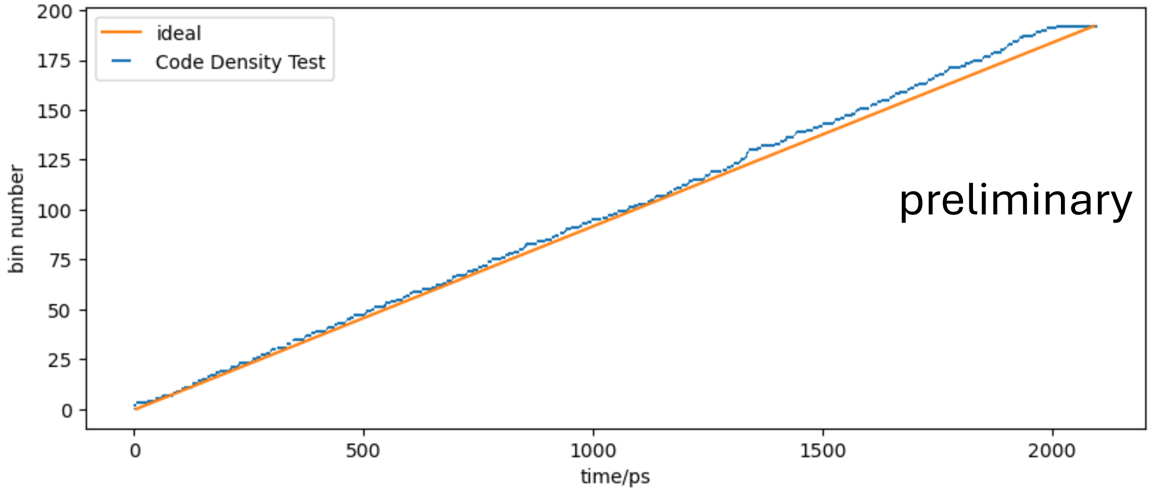
Online Calibration

- An independently generated clock with different frequency will generate signals randomly distributed in time
- The proportion of signals recorded at a TDL stage relative to the total is used to estimate bin width
- Results in calibration table optimised for each channel

$n_{hits} \propto 'time\ width'$



TDL stage



preliminary

Conclusions

- Successfully built powerbase for Hamamatsu M64 that does not require high voltage input
- Assembled at low cost using standard components
- Complimentary readout board being developed using MAROC3A chip
- Time over threshold of sub-nanosecond resolution anticipated using TDL implemented on FPGA
- Aiming for economical light detection system for PMT with proven neutrino physics credentials

Invite Questions

Anthony McCall: Solid Light

Backup Slides

M64 Datasheet

● **GENERAL**

Parameter		Description / Value	Unit
Spectral Response		300 to 650	nm
Wavelength of Maximum Response		420	nm
Photocathode	Material	Bialkali	—
	Minimum Effective Area	18.1 × 18.1	mm^2
Window Material		Borosilicate	—
Dynode	Structure	Metal Channel dynode	—
	Number of Stages	12	—
Anode Size		2 × 2	mm^2
Weight		Approx. 30	g

● **MAXIMUM RATINGS (Absolute Maximum Values)**

Parameter	Value	Unit
Supply Voltage Between Anode and Cathode	1000	Vdc
Average Anode Current in total	0.1	mA

● **CHARACTERISTICS (at 25 °C)**

Parameter		Typical	Unit
Cathode Sensitivity	Luminous (2856 K)	70	μA/lm
	Blue (CS-5-58 filter)	8	μA/lm-b
Quantum Efficiency	(at 420 nm)	20	%
Anode Sensitivity	Luminous (2856 K)	21	A/lm
Gain at 800V		3.0×10^5	—
Anode Dark Current per channel (after 30 min. storage in darkness)		0.2	nA
Time Response (per channel)	Anode Pulse Rise Time	1.5	ns
	Transit Time Spread (FWHM)	0.3	ns
Pulse Linearity per Channel (±5 % deviation)		0.6	mA
Cross-talk (with 1mm Optical Fiber)		2	%
Uniformity among all anodes		1: 3	—

NOTE: Anode characterstics are measured with the voltage distribution ratio shown below.

VOLTAGE DISTRIBUTION RATIO AND SUPPLY VOLTAGE

Electrodes	K	Dy1	Dy2	Dy3	Dy4	Dy5	···	Dy9	Dy10	Dy11	Dy12	P
Ratio	3	2	2	1	1	1 ··· 1		1	1	2	5	

Supply Voltage: 800 Vdc, K: Cathode, Dy: Dynode, P: Anode

Figure 3: Typical Time Response

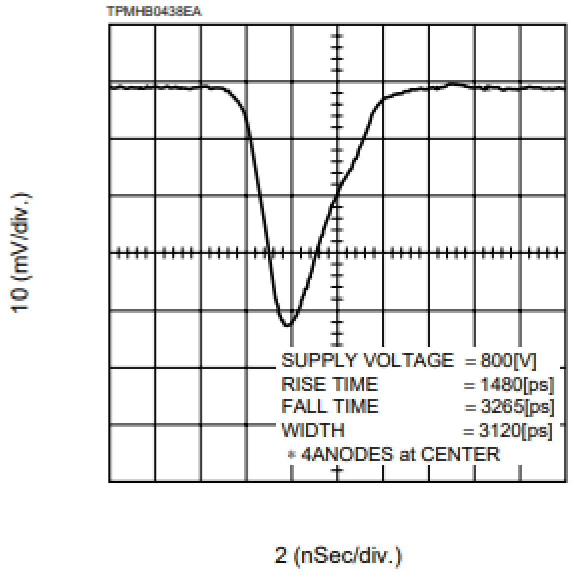
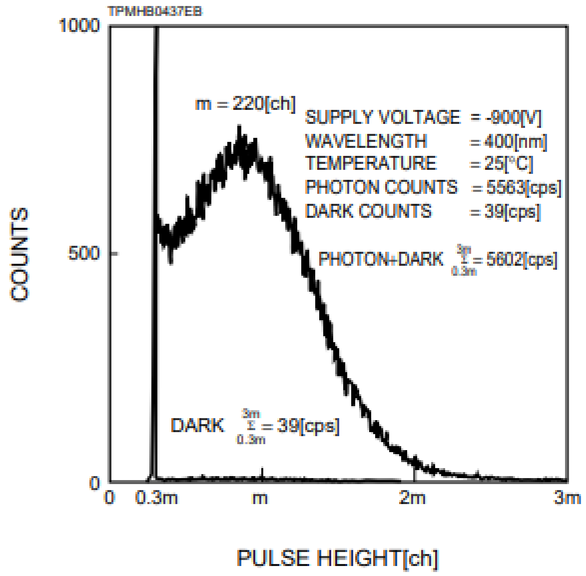
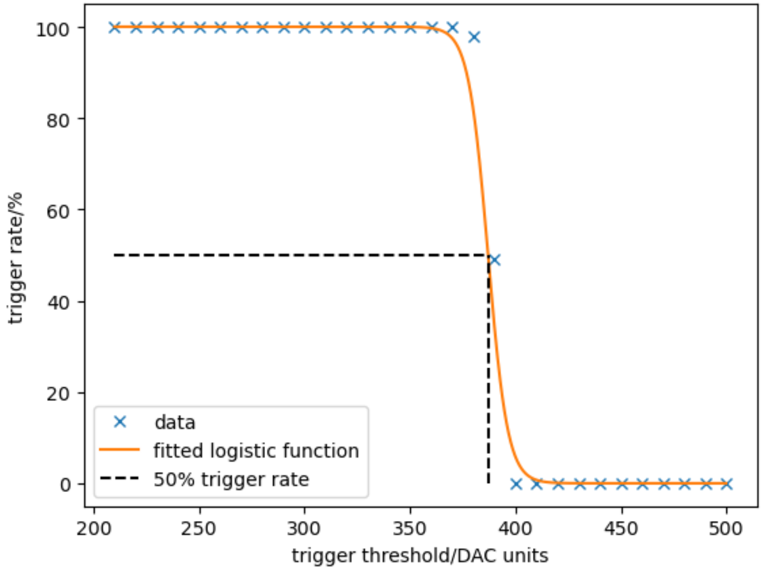


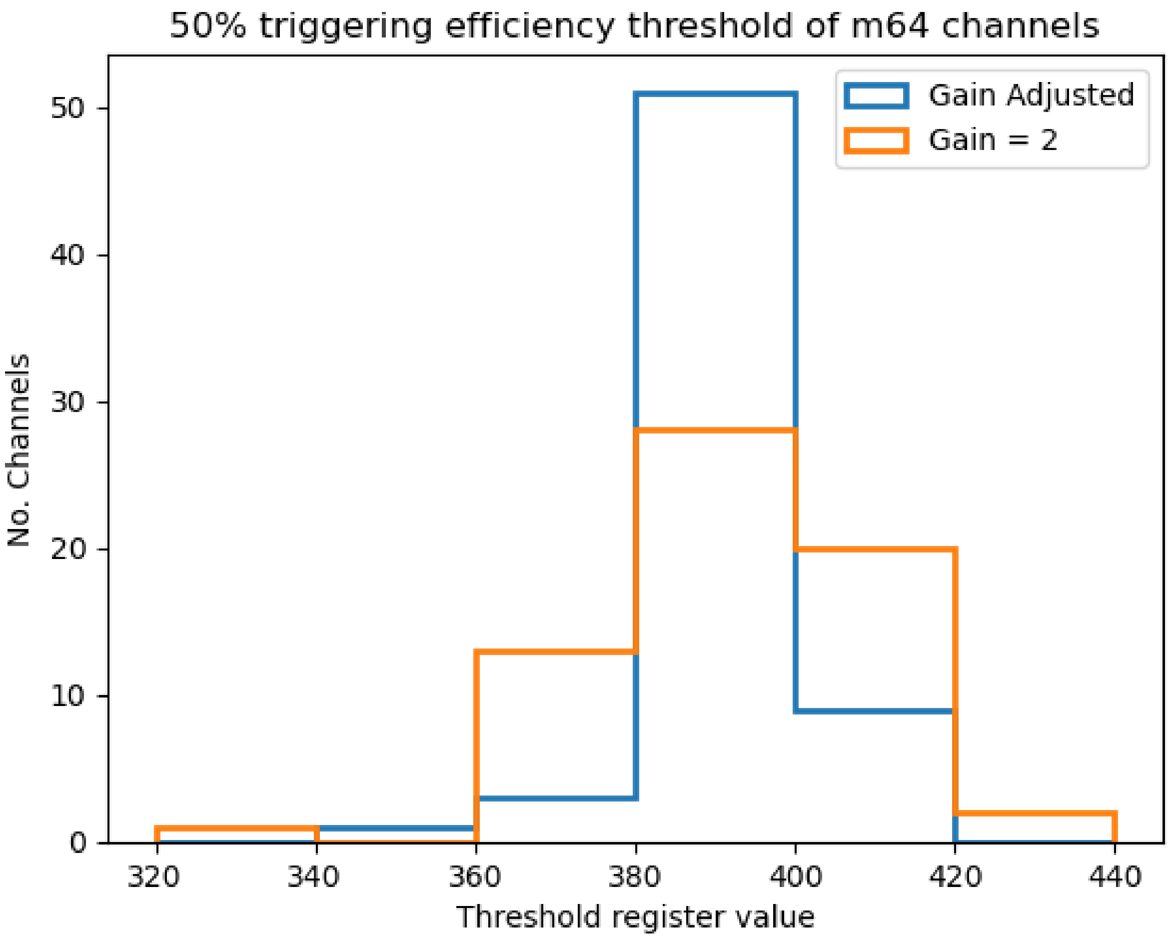
Figure 4: Typical Single Photoelectron PHD



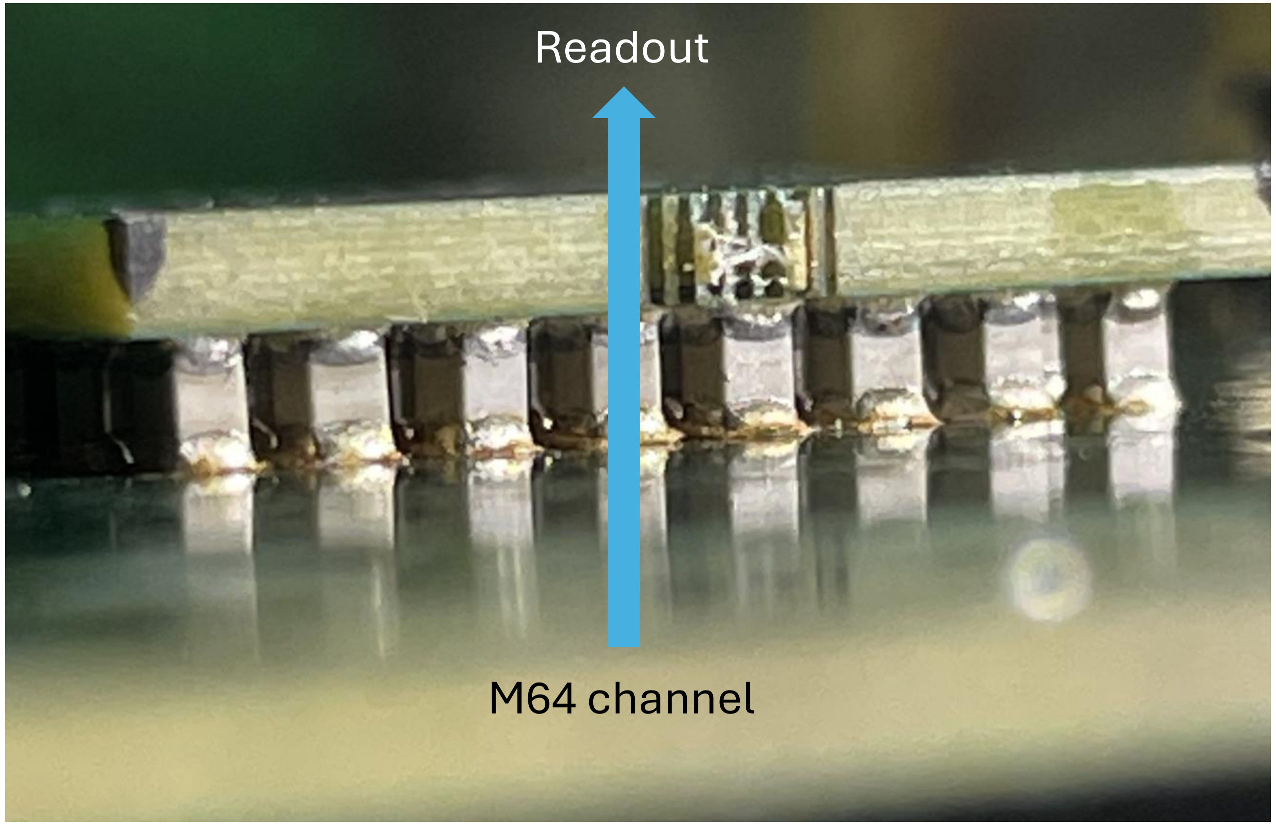
Status of readout

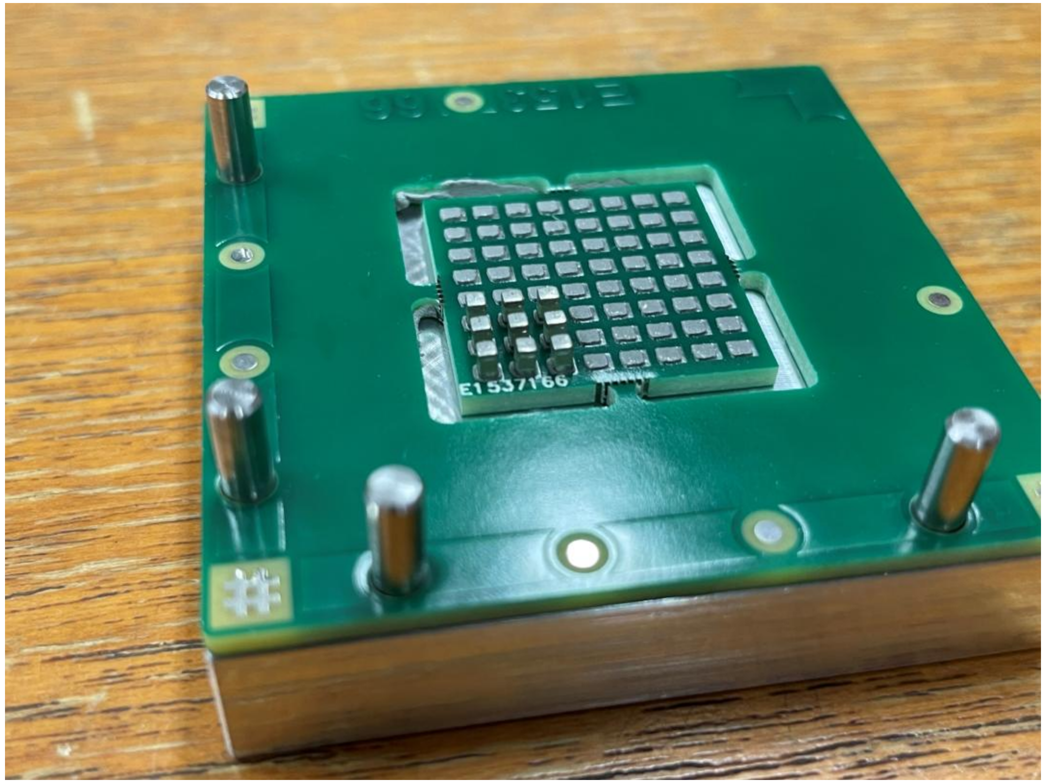
- Gain (amplification) calibration process has been implemented to correct the trigger dispersion of the channels





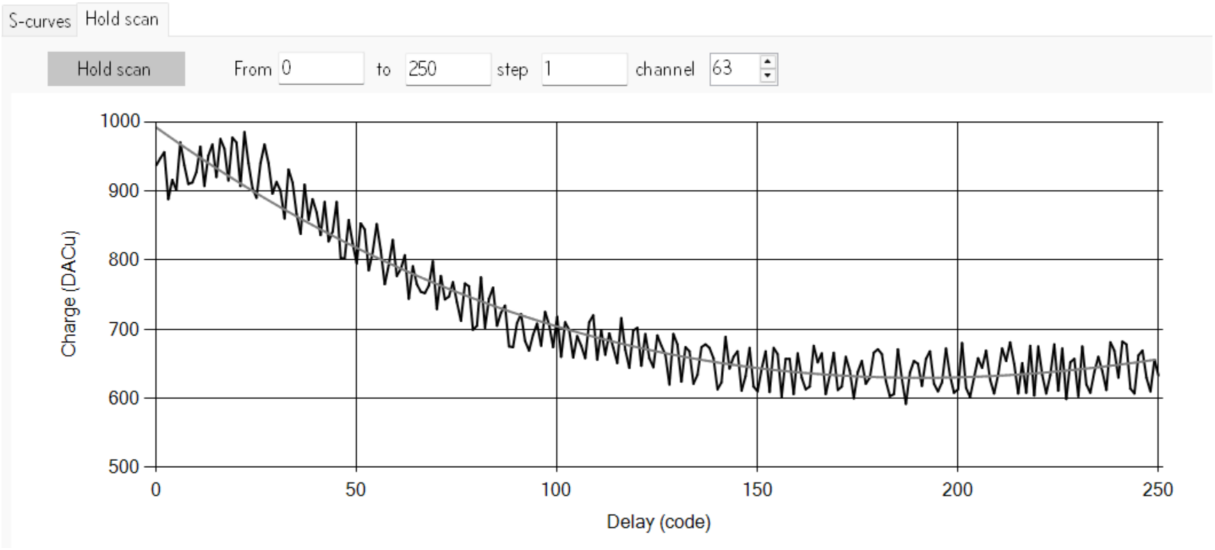
Layout considerations

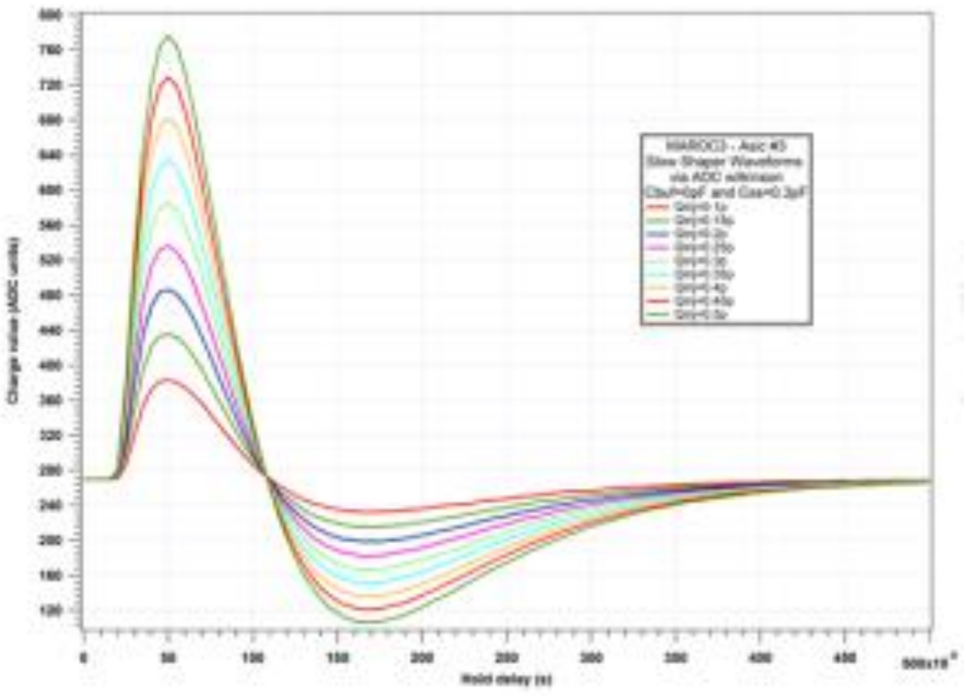


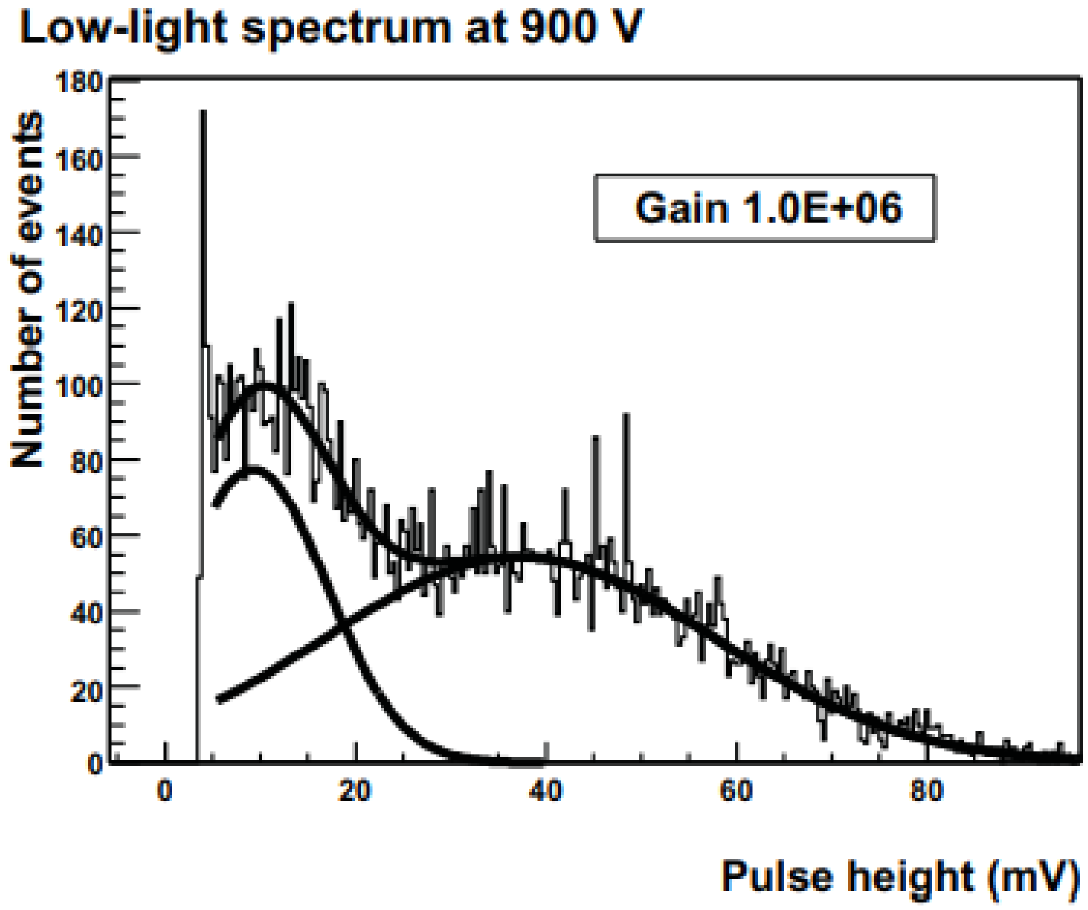


Slow Shaper Waveforms

- Next goal is to calibrate charge ADC readings with known charge inputs
- This requires tuning of Slow Shaper parameters and 'hold' delay

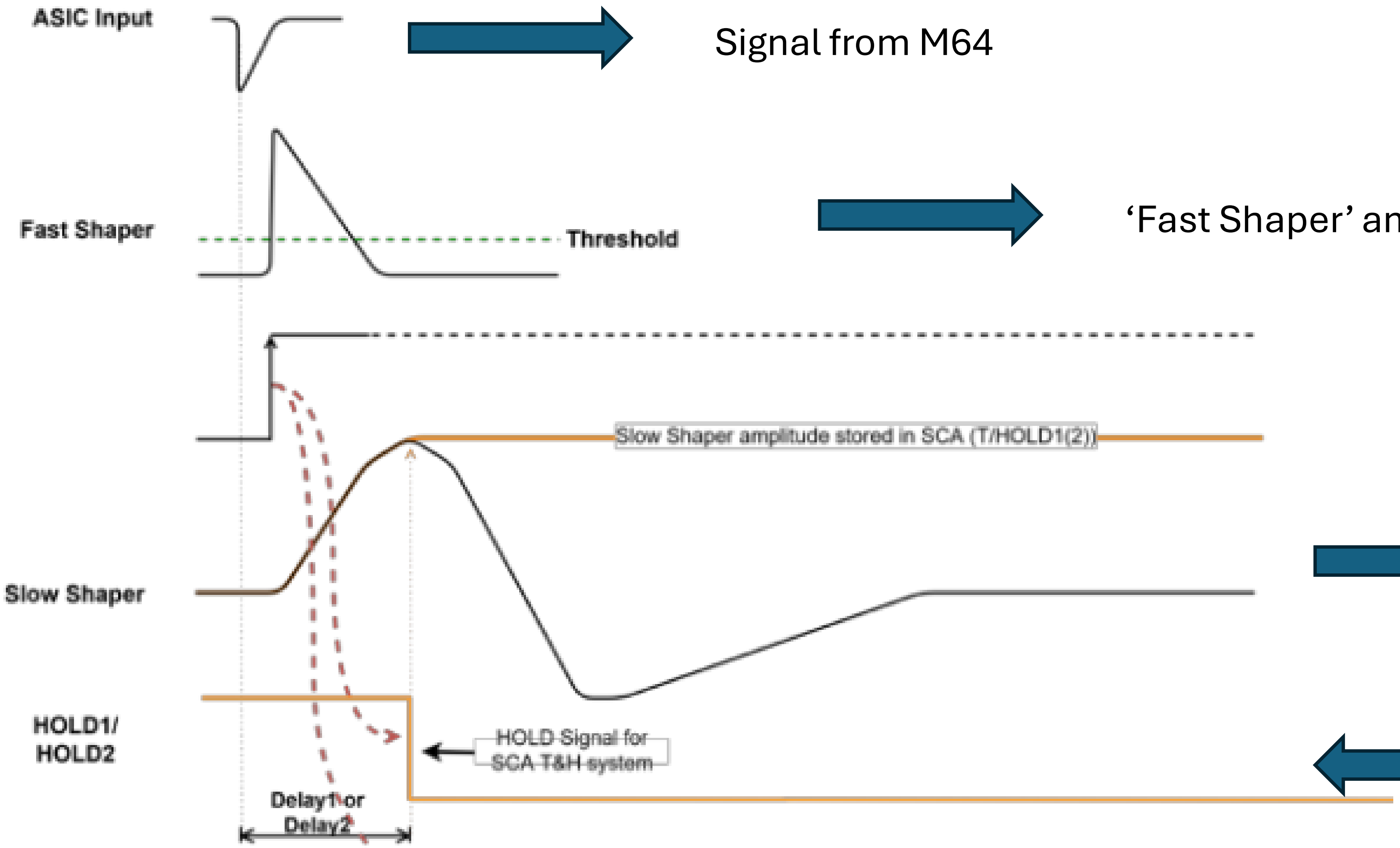






Low-light spectrum at 900 V
Gain 1.0E+06
Number of events
0
20
40
60
80
100
120
140
160
180
0
20
40
60
80
Pulse height (mV)

Readout Design



Signal from M64

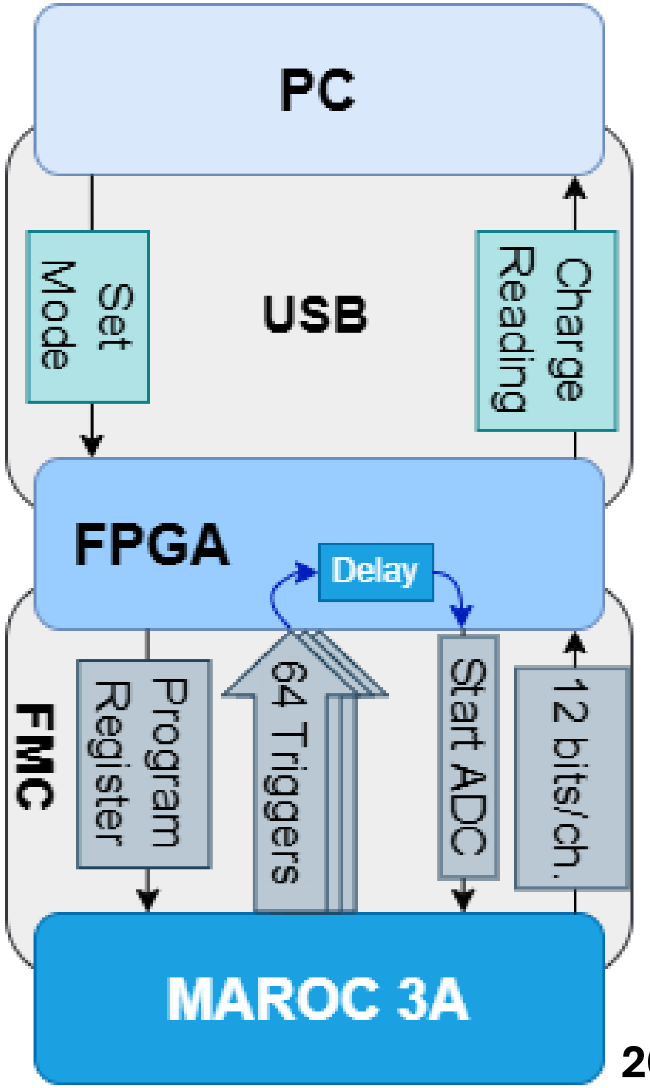
‘Fast Shaper’ amplified for triggering

Simultaneous ‘Slow Shaper’ waveform with variable peaking time

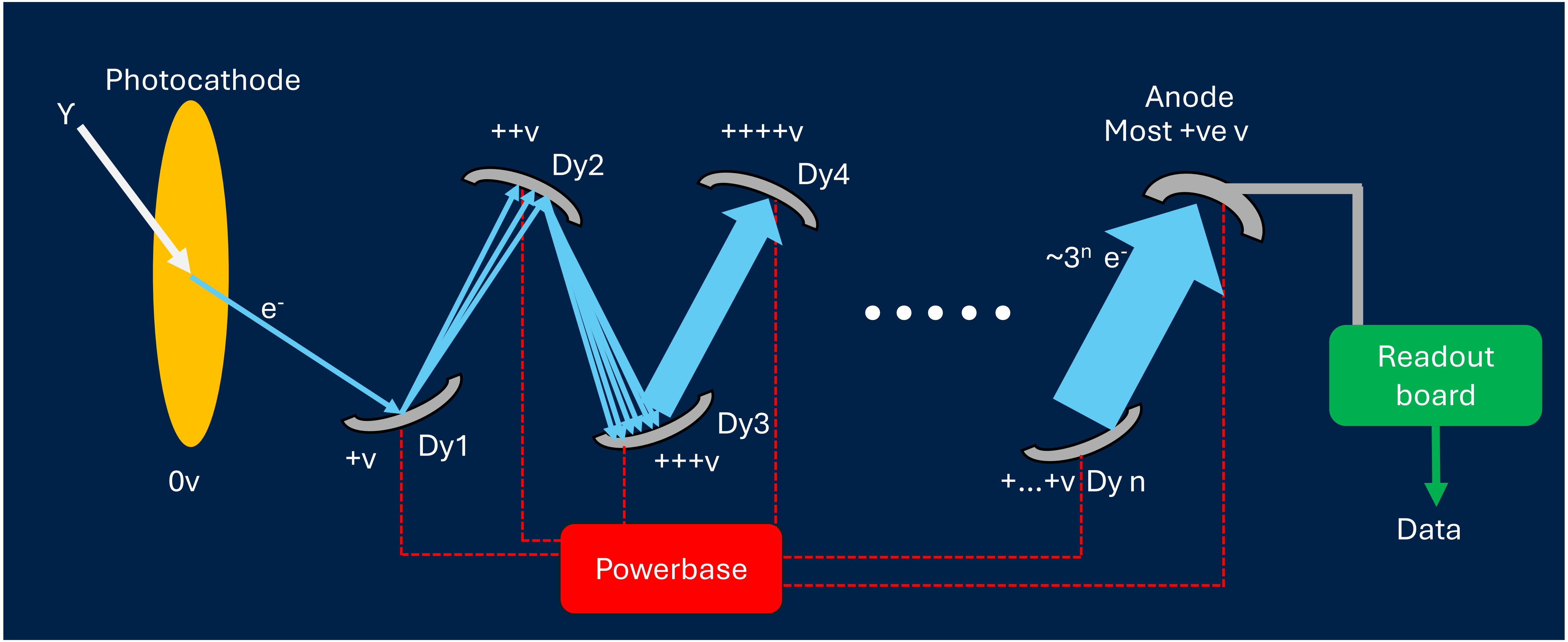
‘Hold’ signal stores amplitude for ADC after user-defined delay following trigger

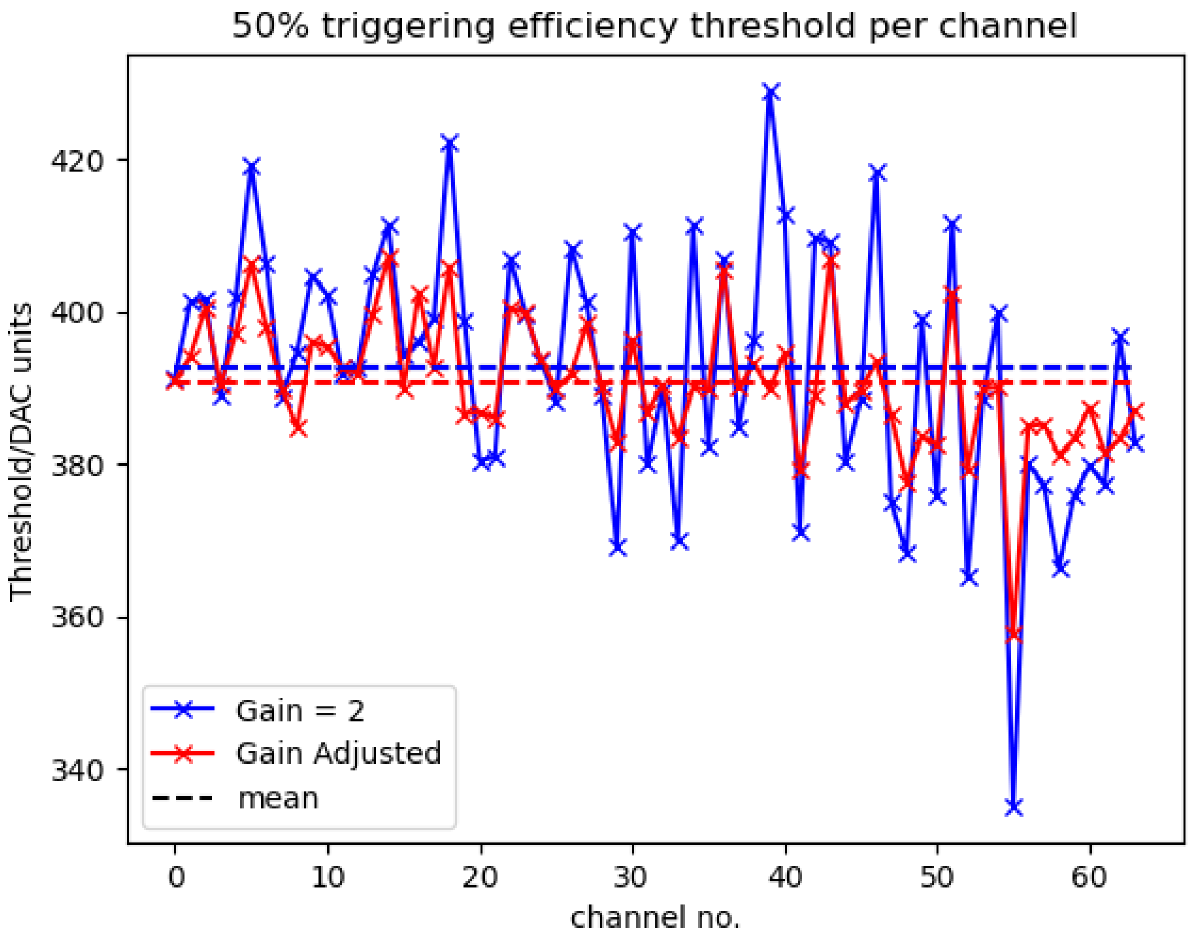
Using the Genesys 2 as an interface

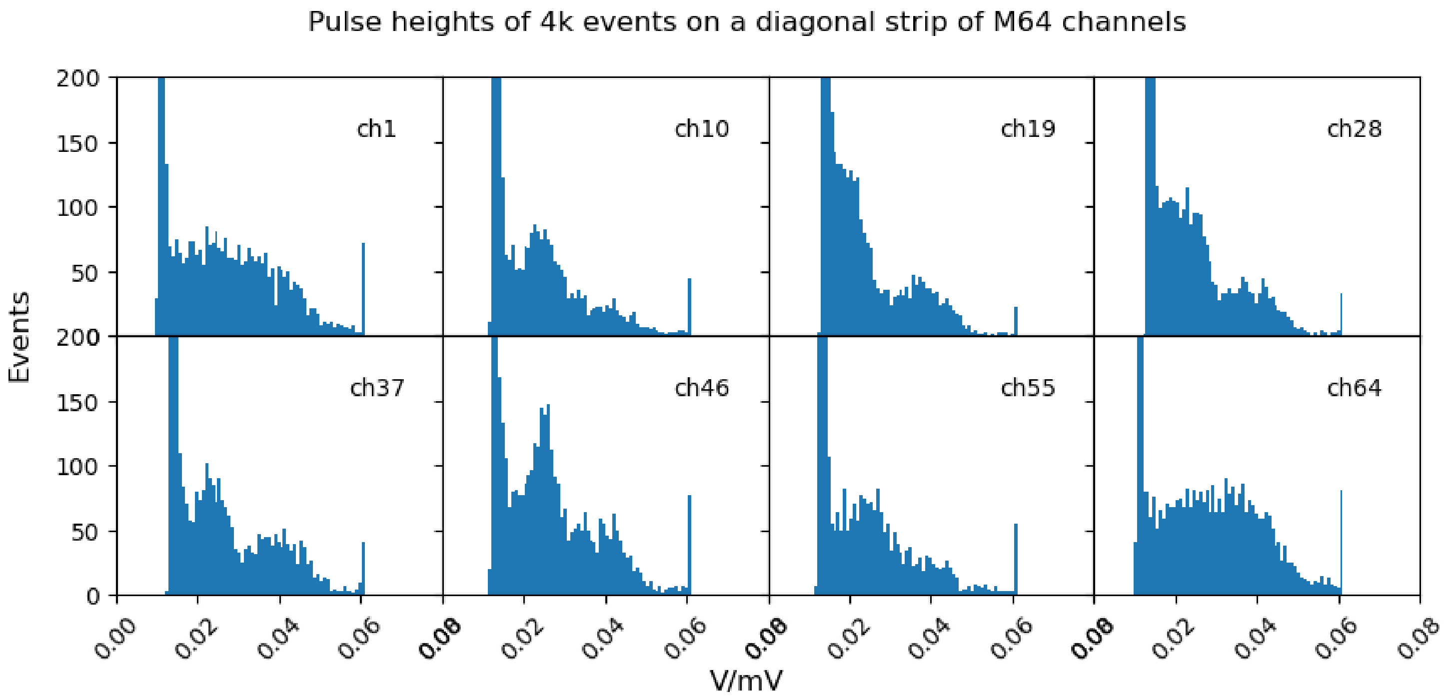
- User interface on computer serially communicates with FPGA to set modes of operation – ‘machine states’
- FPGA programs MAROC with 829 bit register
- MAROC has 64 channel trigger outputs
- FPGA initiates charge measurement process in MAROC based on triggers
- 12 bit ADC measurement for each channel is read by FPGA and transmitted via serial to PC for storage



PMT Principles




50% triggering efficiency threshold per channel
Threshold/DAC units
420
400
380
360
340
0
10
20
30
40
50
60
channel no.
Gain = 2
Gain Adjusted
mean



Pulse heights of 4k events on a diagonal strip of M64 channels
Events
V/mV
ch1
ch10
ch19
ch28
ch37
ch46
ch55
ch64
0
50
100
150
200
0.00
0.02
0.04
0.06
0.08