

ELECTRONICS SIMULATION

Hardware camp 2025 Thanh Sang Lab supporter, Neutrino Lab, IFIRSE, ICISE

LTSPICE INTRODUCTION

I) Powerful, Fast, Free Simulator

2) Using PICE Model

3) Graphical Schematic Capture Interface

4) Supported By Analog Devices

Link Guide: <u>https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator/ltspice-recommended-reading-list.html</u>

Keyboard shortcuts



Common Keyboard

W: wire

Ű.

click

close measure

dialog

Click

click

drag

R: Resistor

C: Capacitor

V: Source

. . . .

- **P**: Pick up components from table
- T: Spice Directive

Crt+R: Rotate component

Almost of cases we use common keyboard

READING COMPONENT DOCUMENTATION AND CHOOSE TYPES OF COMPONENT



NETWORK LABEL

In **LTspice**, a **network label** (or **Net Label**) is a way to assign a custom name to a node in your circuit. This makes the schematic easier to read and allows for easy referencing of signals, especially when working with complex circuits.



SIMULATOR DIRECTIVES — DOT COMMANDS

- Whereas the circuit topology is typically schematically drafted, the commands are usually placed on the schematic as text. All such commands start with a period and are called "dot commands".
- .tran : , and examples...
- .step :
- Syntax: .step param List <value1> <value2> <value3>
- Syntax: .step param <minvalue> <maxvalue> <value_step>
- .text :
- .wave :
- .text :
- .save :

SOURCE AND CURRENT



Functions		DC Value	
(none)		DC value:	
 PULSE(I1 I2 Tdelay Trise Tfall Ton Period Ncycles) 		Make this information visible on schematic:	
◯ SINE(loffset lamp Freq Td Theta Phi Ncy	(cles)		
⊃ EXP(I1 I2 Td1 Tau1 Td2 Tau2)	Small signal AC analysis(.AC)		
◯ SFFM(loff lamp Fcar MDI Fsig)		AC Amplitude:	
) PWL(t1i1t2i2)		AC Phase:	
PWL FILE:	Browse	Make this information visible on schematic: 🚽	
) TABLE(v1 i1 v2 i2)		Parasitic Properties	
I1[A]:	0	This is an active load.	
	10m		
Tdelay[s]:	0	Make this information visible on schematic:	
Trise[s]:	1		
Tfall[s]:	0		
Ton[s]:			
Tperiod[s]:			
Ncycles:			
Additional PWL	Points		
Make this information with a set	a a hamatia.		

Limit current = 10m \Rightarrow Through resistor, voltage drops to 4.95V.

SIMULATION TRACE





For times less than rise delay time, the output current is I_1 . For times between T_{d1} and T_{d2} the current is given by:

 $I_1 + (I_2 - I_1) exp((t - T_{d1})/T_1)$

For times after T_{d2} the current is given by:

$$I_1 + (I_2 - I_1) (exp((T_{d2}-t)/T_2) - exp(T_{d1}/T_1 - t))$$

Name	Description	Units
l1	Initial value	А
12	Pulsed value	Α
Td1	Rise delay time	sec
Tau1	Rise-time constant	sec
Td2	Fall delay time	sec
Tau2	Fall-time constant	sec

SIMULATOR DIRECTIVES — DOT COMMANDS



PREAMPLIER – CHARGE AMPLIER

When a photon hits the SiPM, it triggers an avalanche multiplication process in the microcells, leading to a **flow of charge**. This charge is then detected as a current or voltage signal.

Charge Amplifier:

- + Energy measurement (pulse integration, spectroscopy, low noise).
- + Converts charge (Q) to voltage (V)
- + Stable gain

PREAMPLIER – CHARGE AMPLIER



CHARGE AMPLIFIER SIMULATION



Charge Amplifier $A=C_S/C_f$ C_s : capacitance of signal C_f : capacitance of feedback capacitor

VOLTAGE AMPLIFIER SIMULATION



Simulation result



PEAK DETECTOR



PEAK HOLD SIMULATION





Holding peak

Linearity of holding peak

BACK UP